## REMARKS

Claim 1 is the sole independent claim and stands rejected under 35 U.S.C. § 102 as being anticipated by Yamauchi et al. '503 ("Yamauchi"). This rejection is respectfully traversed for the following reasons.

Claim 1 recites in pertinent part, "a clock supply unit, which respectively ***adjusts the delays of three clock signals*** ... such that the first, the second and the third internal clock signals ***are in phase with each other***" (emphasis added). Yamauchi does not disclose or suggest that the alleged clock supply units 1103, 1105, 1107 shown in Figure 13 have a delay adjustment function. Indeed, the clock signals CK1 outputted from the respective signal generators can be out of phase with each other. As established by law, "inherency may not be established by probabilities or possibilities", *Scaltech Inc. v. Retec/Tetra*, 178 F.3d 1378 (Fed. Cir. 1999).

As anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed, either expressly or inherently, in a single prior art reference, *Akzo N.V. v. U.S. Int'l Trade Commission*, 808 F.2d 1471 (Fed. Cir. 1986), based on the forgoing, it is submitted that Yamauchi does not anticipate claim 1, nor any claim dependent thereon.

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claim 1 is patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable. In addition, it is respectfully submitted that the dependent claims are patentable based on their own merits by adding novel and non-obvious features to the combination.

Based on all the foregoing, it is respectfully submitted that all pending claims are patentable over the cited prior art. Accordingly, it is respectfully requested that the rejection under 35 U.S.C. § 102 be withdrawn.

Regarding new claims 6 and 7, it is respectfully submitted that none of the cited prior art, alone or in combination, disclose or suggest, *inter alia*, the ability for (1) completely stopping the first/second processors and memories; 2) operating only the second processor while accessing the memory; and 3) operating only the first processor while accessing the memory, as can be enabled to be performed by the present invention recited in claims 6 and 7. Indeed, neither Figs. 1-3 of Cai et al. (USP 6,631,474) nor Fig. 6 of Terashima (USP 5,289,436) discloses an integrated circuit having the capability to operate in the aforementioned three modes. Moreover, none of the cited prior art recognizes nor considers such a multi-operational mode capability in a given *combination* of elements defining a device, let alone suggest a means by which to enable such a device.

The Examiner is directed to MPEP § 2143.03 under the subsection entitled "Fact that References Can Be Combined or Modified is Not Sufficient to Establish *Prima Facie* Obviousness", which sets forth the applicable standard:

> The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. (*In re Mills*, 16 USPQ2d 1430 (Fed. Cir. 1990)).

In the instant case, even assuming *arguendo* that the proposed combination can be modified to achieve the claimed invention, it is submitted that the "mere fact that [the proposed combination] can be modified ... does not render the resultant modification obvious" because nowhere does the ***prior art*** "suggest the desirability of the modification" as set forth by the Examiner. Only Applicants have provided the requisite motivation/rationale, and the necessary enablement, to provide such a ***combination*** of elements together to achieve the aforementioned capability.

The Examiner is further directed to MPEP § 2143.03 under the section entitled "All Claim Limitations Must Be Taught or Suggested", which sets forth the applicable standard:

> To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (citing *In re Royka*, 180 USPQ 580 (CCPA 1974)).

In the instant case, the cited prior art does not "establish *prima facie* obviousness of [the] claimed invention" as recited in claims 6 and 7 because the proposed combination fails the "all the claim limitations" standard required under § 103.

## CONCLUSION

Having fully responded to all matters raised in the Office Action, Applicant submits that all claims are in condition for allowance, an indication for which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicant's attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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